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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,576	11/12/2003	Tongbi Jiang	2269-4886.1US (01-0201.01	6662

24247 7590 11/30/2005

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EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/706,576	Applicant(s) JIANG ET AL.
	Examiner Jennifer M. Dolan	Art Unit 2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,365,963 to Shimada (cited by applicant).

Regarding claim 1, Shimada discloses a method for assembling a multi-die package, comprising: providing an interposer (101) with a substantially planar substrate (figures 3-6) and a receptacle (see figure 4a) formed substantially through the substrate, the substrate having an upper and lower surface (figure 4a), the upper surface having conductors thereon (103, 105, 106); positioning at least one first level device (11) within the receptacle (figures 4a-4c), the backside of the device being substantially coplanar with the lower surface of the substrate (figure 4c), an interstitial space remaining between the peripheral edges of the device and the substrate (figure 4c); positioning a second level device (12) above the upper surface of the substrate (figure 4d), a portion of the second-level semiconductor device superimposed with the upper surface of the substrate (see

figures 3 and 6 – the second level device 12 is clearly overlying and partially overlapping the upper surface of the substrate); electrically connecting the first level device to: the conductors on the upper surface of the substrate (i.e. 105 in figure 4d) by first level conductive members (including 111, 104, and 106) that are at least partially carried by the upper surface (wiring pattern 106 is carried on the upper surface of the substrate and connects the via 104 to the right-side pad 105), and electrically connecting the second level device to the conductors on the upper surface by second level conductive members (22). Alternatively, Shimada discloses electrically connecting the first level device to the second level device by first level conductive members (including 111, 104, 105, and 106) that extend between the first and second level devices (collectively, the sequence of traces and vias from 111, 104, 105, and 106 electrically extend between the first and second level devices; see figure 4D).

Regarding claims 2-4, Shimada discloses introducing a quantity of encapsulant material (107) to fill a portion of the interstitial space after electrically connecting the first-level device (column 3, lines 40-55; encapsulant 107 deposited after both chips are connected); and introducing encapsulant between the first and second level devices (figure 4d).

Regarding claims 5 and 6, Shimada discloses positioning intermediate conductive elements between bond pads of the first-level device and interposer conductors (intermediate elements include 21, 111, 104), and between the bond pads of the second level device and the interposer conductors (intermediate elements include 22).

3. Claims 1, 7, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,791,195 to Urushima et al.

Regarding claim 1, Urushima discloses a method for assembling a multi-die package, comprising: providing an interposer (48) having a substantially planar substrate (figure 11a) and a receptacle (51) formed substantially through the substrate (figure 11a), the substrate having upper and lower surfaces with conductors (35) on the upper surface (figure 11a); positioning at least one first-level device (3d) within the receptacle, where the backside is substantially or coplanar with the lower surface of the substrate (figure 11c – the deviation in planarity between the bottom surface of the interposer and the chip is quite small, and hence they are "substantially" coplanar), an interstitial space remaining between peripheral edges of the device and substrate (figure 11a; a portion of 51 remains between device 3d and interposer 48); positioning a second level device (3c) above the upper surface of the substrate (figure 11a), a portion of the second level device superimposed with the upper surface of the substrate (figure 11a- device 3c clearly is disposed on and partially overlaps the interposer); electrically connecting the first level device to the second level device by first level conductive members that extend between the first and second level devices (first and second level devices are connected through the solder bump carried by the first level device 3d); and electrically connecting the second device to the conductors on the upper surface of the substrate by second level conductive members (through bumps 21 carried by the second level device 3d between the device and the interposer).

Regarding claim 7, Urushima discloses positioning the second level device in a flip-chip arrangement over the first level device; and positioning the second level device over the interposer (figure 11a).

Regarding claim 8, Urushima discloses securing the first and second level devices to one another before positioning the second device (figure 11b; column 20, lines 10-30).

4. Claims 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,949,135 to Washida et al. (cited by applicant).

Regarding claim 18, Washida discloses providing an interposer (701) with a substantially planar substrate (figure 1) and a receptacle (701a) formed through the substrate; positioning a first semiconductor device (760) over a first (lower surface; see figure 1 – since the chip is disposed at a level lower than the bottom surface of the interposer, it is considered to be "over" that surface) surface of the interposer, at least one bond pad (763) being exposed to the receptacle (figure 1); positioning a second device (750) over a second surface (top in figure 1) of the interposer, at least one bond pad (753) of the second device being exposed to the receptacle (figure 1); and electrically connecting the bond pads through the receptacle (figure 1).

Regarding claim 19, Washida discloses securing a conductive structure (either 707 or 706) to the bond pads of the second device (figure 1).

Regarding claim 20, Washida discloses that the securing of conductive elements (707) is effected before positioning (column 4, lines 50-65).

Regarding claim 21, Washida discloses that the securing of conductive elements (706) to the structure is effected after positioning (column 5, lines 1-20).

5. Claims 18, 19, 21, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,441,495 to Oka et al.

Regarding claim 18, Oka discloses providing an interposer with a substantially planar substrate (1a; figure 17, 18, 20, 23) and a receptacle formed substantially through the substrate (12a); positioning a first device (2c) over a first surface of the interposer, at least one bond pad (23, 24) being exposed to the receptacle (figure 17); positioning a second device (2d) over a second surface of the interposer, at least one bond pad (22a) being exposed to the receptacle (figure 17); and electrically connecting the bond pads through the receptacle (figure 17; column 13, lines 15-55).

Regarding claims 19 and 21, Oka discloses that conductive structures 22a and 23 are secured to the bond pad of the opposite chip after positioning (column 13, lines 15-55).

Regarding claim 22, Oka discloses that the first device comprises a portion of a redistribution circuit (see column 13, lines 55-67; figures 17-18).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6 and 9-12 are rejected under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 6,452,278 to DiCaprio et al. (cited by applicant) in view of U.S. Patent No. 6,469,395 to Nishihara et al. (cited by applicant).

Regarding claim 1, DiCaprio discloses a method for assembling a multi-die package, comprising: providing an interposer (14) having a substantially planar substrate (figures 3, 4) and a receptacle formed substantially through the substrate (see figures 6a-6c; column 2, lines 23-27), the substrate having upper and lower surfaces, wherein the upper surface has conductors thereon (portion of bond fingers 16 connected over vias 22; figures 1-4); positioning at least one first level device (12) within the receptacle (figures 6a-6c; column 2, lines 23-28), a backside of the first level device being substantially coplanar with the lower surface of the substrate (figures 1-4), an interstitial space remaining between the peripheral edges of the device and the receptacle (figures 1-4; 6a-6c); positioning a second level device (42, 50, or 58) above the upper surface of the substrate (figures 2-4; second level device is 'above' the substrate); and electrically connecting the first level device to the conductors on the upper surface of the substrate by first level conductive members (wirebond 24 and bonding finger portion of 16 receiving the bonding wire) at least partially carried by the upper surface (bonding finger portion of 16 is clearly carried by the upper surface of the substrate; also see column 2, lines 42-58); and electrically connecting the second level device to conductors on the upper surface of the substrate by second level conductive members (upper wirebond 24; see figures 3 and 4).

DiCaprio, however, only explicitly teaches second level devices having the same size as and superimposed on the first level device. Hence, there is no teaching of using a

larger second level semiconductor device that at least partially superimposes the upper surface of the substrate.

Nishihara discloses a packaging structure substantially similar to that of DiCaprio, including an interposer (6a), a first level device (2a) disposed within a receptacle in the interposer and including a similar wirebonding configuration extending from the top of the first level device to the top of the interposer (see figure 3), and a second level device (2b) disposed above the interposer and first level device, the second level device at least partially superimposing the top surface of the interposer (see figure 3 – the second level device partially overlaps with the interposer).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of DiCaprio, such that second level chips larger than the first level chips, and hence superimposed partially with the upper surface of the substrate, may be used, as suggested by Nishihara. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use larger second level devices that partially superimpose the interposer surface, because it is apparent that the interposer, first level device, and first level wirebond structures of DiCaprio (from figure 4) and Nishihara (from figure 3) are substantially similar, and hence, it is apparent that the configurations of the second level devices in DiCaprio and Nishihara are reasonably considered interchangeable. Since Nishihara shows that a very large second level device may be disposed on the first level device without interfering with the wirebonding structure, without requiring disposition of a thick spacer layer between the first and second level devices, and without requiring a second level bonding wire by simply using a ball grid type second level device (see Nishihara, figure 3 and column 4,

lines 1-46), a person having ordinary skill in the art would find such an arrangement advantageous for the elimination of these complex and restrictive manufacturing steps. Additionally, a person having ordinary skill in the art would recognize that the use of larger second level chips provides the advantages of increased compatibility of the package structure with all chip types and sizes, and improved device density relative to the overall footprint of the package.

Regarding claims 2 and 3, DiCaprio discloses introducing encapsulant to fill at least a portion of the interstitial space (column 2, lines 14-24; figures 1-4), where the encapsulation occurs after forming the electrical connections (see figures 6c-6d; wirebonding must inherently occur before encapsulation).

Regarding claim 4, DiCaprio discloses introducing epoxy, which is an encapsulant-type material, between the first and second level devices (column 3, lines 30-35).

Regarding claims 5 and 6, DiCaprio discloses forming intermediate conductive elements (wirebonds 24) between the bond pads of the first and second level devices and the conductors of the interposer (figures 3 and 4).

Regarding claims 9 and 10, DiCaprio discloses providing a multi-interposer substrate (figure 7), which is singulated into individual assemblies (column 2, lines 20-23; column 4, lines 1-10).

Regarding claims 11 and 12, DiCaprio discloses adhering a film (70) to the lower surface of the substrate to cover a portion of the receptacle (column 4, lines 10-20) prior to the positioning of the first device therein (figures 6a-6b), and removing the adhered

film from the lower surface following curing of the encapsulant in the receptacle (column 4, lines 20-30; figures 6d-6f).

8. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima in view of U.S. Patent Publication No. 2002/0047214 to Morinaga et al.

Urushima fails to disclose another first level device within the receptacle, where the first-level devices are back-to-back, where the 'another' first level device has bond pads connected to conductors on the lower surface of the interposer.

Morinaga discloses that two first level chips (6a and 6b) may be stacked back-to-back in a receptacle in the interposer (figure 5), where the 'another' first level chip is electrically connected to conductors (43) on the lower side of the substrate (figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Urushima, such that in place of the single chip in the receptacle, two first-level back-to-back chips are disposed in the receptacle, each chip being electrically connected to the nearest surface of the interposer, as suggested by Morinaga. The rationale is as follows: A person having ordinary skill in the art would have been motivated to dispose both chips in the receptacle, because doing so allows multiple same-sized chips to be packed in a small area, such that a reduced profile is achieved, and such that bonding wires connecting the chips to the interposer do not interfere with each other (see Morinaga, figure 5; paragraphs 0030-0034; 0044).

9. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima in view of Morinaga, as applied to claim 13 above, and further in view of U.S. Patent No. 6,388,333 to Taniguchi et al.

Urushima fails to teach a third-level device over the lower surface of the substrate.

Taniguchi discloses that interposers may be double-sided, such that devices are disposed in a substantially similar manner over both the top and bottom surfaces of the interposer (see figures 19, 33; column 14, lines 20-55), where the devices disposed on the bottom surface of the interposer are connected to the conductors on the lower surface of the interposer and where chips on both sides of the interposer are electrically connected to each other (figure 19; column 14, lines 20-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Urushima as modified by Morinaga, such that the interposer is double-sided, with similar device structures attached to each side (i.e., a third device analogous to the second level device formed below the interposer, where the third device and 'another' first level device are interconnected, analogous to the connections between the first level device and second level device, and where the third level device is connected to the lower side of the interposer, analogous with the second level device being connected to the upper side of the interposer), as suggested by Taniguchi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a double-sided interposer, with 'mirrored' device structures on each side, because Taniguchi shows that such a stacking minimizes the total device height of the structure per chip on the interposer (Taniguchi, compare figure 18 with

figure 19 or the bottom embodiment in figure 33 with any of the other embodiments), minimizes the length and mutual interference of wirebonds (Taniguchi, compare figure 18 with figure 19), and minimizes the required number of stacked interposers per chip in the module (Taniguchi, figure 33).

10. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiCaprio et al. in view of Nishihara et al., as applied to claim 1, supra, and further in view of Morinaga et al.

DiCaprio as modified by Nishihara fails to disclose another first level device within the receptacle, where the first-level devices are back-to-back, where the 'another' first level device has bond pads connected to conductors on the lower surface of the interposer.

Morinaga discloses that two first level chips (6a and 6b) may be stacked back-to-back in a receptacle in the interposer (figure 5), where the 'another' first level chip is electrically connected to conductors (43) on the lower side of the substrate (figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of DiCaprio as modified by Nishihara, such that in place of the single chip in the receptacle, two first-level back-to-back chips are disposed in the receptacle, each chip being electrically connected to the nearest surface of the interposer, as suggested by Morinaga. The rationale is as follows: A person having ordinary skill in the art would have been motivated to dispose two chips in the receptacle, because doing so allows multiple same-sized chips to be packed in a small area, such that a reduced profile is achieved, and such that bonding wires connecting the chips to the

interposer do not interfere with each other (see Morinaga, figure 5; paragraphs 0030-0034; 0044), and furthermore, the combination of DiCaprio and Morinaga would enable the connection of 3 chips on the module without significantly increasing the height profile of the structure (Morinaga, figure 5; DiCaprio, figures 3 and 4).

11. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiCaprio et al. in view of Nishihara et al. and Morinaga, as applied to claim 13 above, and further in view of U.S. Patent No. 6,388,333 to Taniguchi et al.

DiCaprio fails to teach a third-level device over the lower surface of the substrate.

Taniguchi discloses that interposers may be double-sided, such that devices are disposed in a substantially similar manner over both the top and bottom surfaces of the interposer (see figures 19, 33; column 14, lines 20-55), where the devices disposed on the bottom surface of the interposer are connected to the conductors on the lower surface of the interposer and where chips on both sides of the interposer are electrically connected to each other (figure 19; column 14, lines 20-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of DiCaprio as modified by Nishihara and Morinaga, such that the interposer is double-sided, with similar device structures attached to each side (i.e., a third device analogous to the second level device formed below the interposer, where the third device and 'another' first level device are interconnected, analogous to the connections between the first level device and second level device, and where the third level device is connected to the lower side of the interposer, analogous with the second level device being connected to the upper side of the interposer), as

suggested by Taniguchi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a double-sided interposer, with 'mirrored' device structures on each side, because Taniguchi shows that such a stacking minimizes the total device height of the structure per number of chips held (Taniguchi, compare figure 18 with figure 19 or the bottom embodiment in figure 33 with any of the other embodiments), minimizes the length and mutual interference of wirebonds (Taniguchi, compare figure 18 with figure 19), and minimizes the required number of stacked interposers per chip in the module (Taniguchi, figure 33).

Response to Arguments

12. Applicant's arguments filed 9/6/05 have been fully considered but they are not fully persuasive.

Regarding the 35 U.S.C. 112 rejection, the Applicant's arguments are persuasive, and the rejection has been dropped.

Regarding the rejections based on Washida, the Applicant argues that the second level device is not superimposed with the interposer substrate and that the lower semiconductor device 760 is positioned at least partially within the hole in the interposer, and thus, is not positioned over the surface of the interposer.

The Examiner agrees with the Applicant's characterization that the second level device is not superimposed with the interposer. Thus, the rejections of claims 1 and 5-8

based on Washida have been withdrawn. The Examiner, however, respectfully disagrees with the arguments relating to claims 18-21. The Applicant nowhere discloses or claims positioning the devices such that they are directly overlying or supported by the surfaces of the interposer. Hence, "over" is given its broadest reasonable interpretation, which is that the device is simply positioned at a level at least partially higher than the surface of the substrate. It is immaterial whether the device is partially within the hole. Also, this interpretation of "over" is supported by the claim language of claim 18 taken in conjunction with the language of dependent claim 20. Claim 20 requires that the bond pads of the first and second devices be secured to each other before the first device is positioned over the first surface of the substrate and the second device is positioned over the second surface of the substrate. However, figure 9 and paragraph 0078, which is the only disclosed embodiment of the invention that reads on claim 18 as the Applicant appears to interpret the claim (see pages 9-10 of Applicant's remarks) cannot physically meet the terms of claim 20, since at least one of the semiconductor devices in the embodiment of figure 9 must be connected to the interposer substrate before the two devices can be electrically connected through the receptacle. Since the only disclosure (and apparently the only physically realizable situation) of securing the two devices before positioning either device relative to the interposer corresponds to at least one of the devices being smaller than the aperture and positioned through the aperture (akin to figures 7 or 8), the Examiner is forced to make a liberal interpretation of "over" in light of the specification to meet the conditions of claim 20.

Regarding the rejections based on Shimada, the Applicant argues that Shimada does not disclose connecting the first chip to electrode pads on the upper surface of the substrate by way of a conductive member that is at least partially carried by the upper surface of the substrate, and that Shimada does not expressly or inherently disclose connecting the first chip to the second chip.

This is not persuasive, because Shimada discloses that the chip 11 is connected to the wiring pattern 111 through the solder balls 21 and internal wiring pads 112 (see column 3, lines 25-35), the wiring pattern connects to wiring patterns 105 and 106 through vias 104 (column 3, lines 10-25). Since any portion of elements 105 and 106 can be taken as the conductive member on top of the interposer substrate, then any portion of 105 and 106 connected between that designated portion and the vias can be considered to be the first level conductive member carried upon the upper surface of the interposer. It is also apparent that the device 11 must inherently have an electrical connection between either the external ball bonds 13 or to the second level device 12 in order to function, as would be apparent to a person having ordinary skill in the art. The Examiner further respectfully points out that the alternative language in line 14 of claim 1, (i.e., "electrically connecting...to at least one of:") only requires connection to either the conductor on the upper surface of the substrate or to the second level device, and not to both of these structures. Hence, Shimada anticipates the claims for at least the reasons above. Alternatively, the Examiner also respectfully points out that figure 6 clearly illustrates a connection between the first chip, the lower wiring pattern, the vias 104, and a pad connecting to the second chip (either of the pads connected to the second-level wirebonds 108), and thus appears to meet the alternative condition of claim 1.

Regarding the rejections using DiCaprio, the Examiner agrees with the Applicant's argument that DiCaprio does not teach a second level die that superimposes at least part of the interposer substrate, as required in the 9/6/05 amendment to the claims. The 35 U.S.C. 102 rejections over DiCaprio have been withdrawn and replaced by 35 U.S.C. 103 rejections supplying the missing claim elements.

Regarding the rejections using Oka, the Applicant argues that Oka discloses a TAB substrate, which is not an interposer.

This is not persuasive, because Oka teaches the use of a carrier substrate comprising any of a thin resin substrate, a lead frame, or a "plate-type" substrate having conductive traces (see column 2, lines 40-55; column 3, lines 1-15), wherein the substrate is used as an intervening or interposing element between chips and a lower-level substrate (see column 12, line 40 – column 13, line 10). Hence, the structure disclosed by Oka meets the literal definition of an interposer. Additionally, since the structure of Oka is not dissimilar to the structures disclosed by the Applicant (figure 9 shows a 'flex substrate' structure, which is substantially similar to the thin resin substrate of Oka; figures 6-8 show substrates substantially similar to the plate substrate of Oka, both the substrates of Oka and the substrates disclosed by the Applicant are used to connect the chips to a lower level wiring board through solder balls (see Oka, column 12, line 40 – column 13, line 10), the Examiner considers the structure disclosed by Oka to be substantially similar to, and hence, not patentably distinct from, that defined in claim 18.

Regarding the rejections using Urushima, the Applicant argues that the backside of the first level device in Urushima is not substantially coplanar with a surface of the interposer, but rather, the backside is located in a plane beneath the interposer.

This is not persuasive, because the Applicant has not established in the specification a range of values by which the term "substantially" is to be interpreted, the term is considered to have the meaning of "approximately" or "nearly", or "generally," rather than having the meaning of "exactly." Hence, since the deviation between the lower surface of the first level device and the lower surface of the interposer is quite small in Urushima, they are considered to be "substantially coplanar."

Regarding the arguments pertaining to the combination of Urushima and Morinaga, the Applicant argues that the teachings of Urushima are limited to assembling a first level device such that the backside of the device is located outside of the plane of the interposer, and hence, any additional first level devices could not be located in the hole.

This is not persuasive, because Urushima does not provide any guidance as to the desired or required locations of the backside of the first level device. Since the rejection looks to Morinaga and not Urushima for the teachings of placing the backside of the first level device at the center plane of the interposer, it is not particularly relevant where Urushima places the backside of the first level device. Furthermore, since the first level device of Urushima is placed in the hole by virtue of connection to the second level devices rather than through any specific connection to the interposer, it would be reasonable for a person having ordinary skill in the art to expect that a thinner first level

device can be placed in the hole in the same manner taught by Urushima without actually affecting the structure or the packaging method of the structure.

Conclusion

13. Applicant's amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

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